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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,163	12/29/2000	Salvatore N. Storino	RO998-200B	1259

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EXAMINER
NGUYEN, KHIEM D

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 09/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/751,163	Applicant(s) STORINO ET AL.	
	Examiner Khiem D Nguyen	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with th correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-16* is/are allowed.

6)☒ Claim(s) *1-6 and 17-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Terminal Disclaimer

The terminal disclaimer filed on 02-25-2003 is proper and has been recorded. The final rejection as set forth in paper No. (5) is withdrawn. A new rejection is made as set forth in this Office Action.

Claims (1-21) are pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

1. Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Bosshart (U.S. Patent 6,049,231).

In re claim 1, Bosshart discloses a method of eliminating parasitic bipolar transistor action in a Silicon on Insulator (SOI) Metal Oxide Semiconductor (MOS) device located in a logic circuit, the logic circuit being adapted to receive an input signal and a clock signal, the method comprising: controlling the conduction of an active discharging device with the input signal (FIG. 4, $INPUTS_{26}$) wherein the discharging device (FIG. 4, 26_{DT}) being coupled to an intermediate node of the logic circuit (FIG. 4,

26_L), whereby the parasitic bipolar transistor is deactivated (col. 8, line 53 to col. 10, line 17).

In re claims 2-6, Bosshart discloses wherein the SOI device comprises a gate and a drain, and wherein the method further comprises: providing a first signal (FIG. 4, $INPUTS_{26}$) to the gate of the SOI device, providing a second signal to the drain of the SOI device, and activating the conduction of the active discharging device according to the state of the first signal wherein the first signal causes the SOI device to conduct current whenever the logic circuit is being pre-charged and the second signal pre-charges the drain during a pre-charge cycle and wherein the active discharging device provides a conduction path between the intermediate node and a voltage source (col. 8, line 53 to col. 10, line 38 and FIG. 4)

2. Claims 17-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Bosshart (U.S. Patent 6,049,231).

In re claim 17, Bosshart discloses a method of reducing the effects of parasitic bipolar transistor action in a silicon-on-insulator (SOI) logic circuit during a pre-charge cycle, comprising: coupling an active discharge device to an intermediate node of the SOI logic circuit, and controlling the conduction of the active discharging device using a non-clock signal whereby the charge at the intermediate node is maintained at a predetermined level during the pre-charged cycle (col. 8, line 53 to col. 10, line 17 and FIG. 4).

In re claims 18-21, Bosshart discloses wherein the predetermined level is a common ground potential for the SOI logic circuit and wherein the non-clock signal

comprises an active low signal applied to an input of the SOI logic circuit during the pre-charge cycle. Bosshart also discloses wherein the voltage source comprises a system ground (col. 8, line 53 to col. 10, line 38 and FIG. 4).

Allowable Subject Matter

Claims 7-16 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (703) 306-0210. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-9179 for regular communications and (703) 746-9179 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
July 12, 2003

Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800